Validation of a Nonlinear Transistor Model by Power Spectrum Characteristics of HEMT's and MESFET's

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***Abstract*—The bias dependence of the power output spectrum and the generation of intermodulation products from different HEMT's and MESFET's at large signal excitation is studied and compared with simulated values. An extended HEMT/FET model suitable for small and and negative V_{ds} (with a drain voltage dependence of the peak transconductance in the unsaturated drain current region, and at negative drain voltage), is also proposed. Good agreement between simulated and measured power spectrum up to at least the fourth harmonic is demonstrated for HEMT and MESFET devices from different manufacturers. Measured and simulated intermodulation products are also in good agreement, which confirm the validity of the model.**

I. Introduction

NONLINEAR simulation of active circuit is an important tool when designing frequency translators (mixers, harmonic generators), attenuators, oscillators and power amplifiers [1]–[15]. Generation of unwanted spuriouses (intermodulation, generation of harmonics), saturation effects in amplifiers, mixers and oscillators, and phase noise in oscillators are some examples of parameters that have to be considered. The quality of the model can be measured in different ways: comparision of measured and simulated I-V characteristics [4], two dimensional simulations, RF load-pull measurements, or comparision of measured and simulated bias dependent S-parameters [1]–[3], [5]. Recently, pulsed S-parameters [14] and power spectrum analysis [6], [7], [9], [10], [15] has been used in the parameter extraction.

Our model [11] has been found to be suitable for modeling MESFET- and HEMT-based circuits, such as frequency doublers [16] and drain mixers [17]. The drain current and its derivatives were well described by this model. This makes it possible to correctly simulate the generated intermodulation products, since the derivatives determine the intermodulation levels [6]. The object of this paper is to increase the drain voltage range in which the model of the drain current I_{ds} [11] is valid and to validate the feasibility of this model to predict output power spectrum characteristics and intermodulation. Measured and simulated gate and drain voltage dependent DC-characteristics and power spectrum at four harmonics and at different input powers are compared, as well as the generation of intermodulation products by two-tone excitation.

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II. Device Modeling

The equation for the drain current of a FET device in our model is [11]

$$I_{ds} = I_{pk}(1 + \tanh(\psi))(1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \quad (1)$$

where I_{pk} is the current and V_{pk} is the gate voltage for peak transconductance, λ is the channel length modulation parameter, and α is the saturation voltage parameter. The parameters of the drain part, α and λ, are the same as those used in the modified Materka model [18], [19]. Ψ is a power series function centred at V_{pk} with variable V_{gs}, i.e.

$$\psi = P_1(V_{gs} - V_{pk}) + P_2(V_{gs} - V_{pk})^2 + P_3(V_{gs} - V_{pk})^3 + \cdots. \quad (2)$$

As a first approximation $P_1 = P_{1sat} \approx g_{ms}/I_{pks}$, where g_{ms} and I_{pks} are measured in the saturation region. For some devices it is difficult to define the gate voltage V_{gs} at which the transconductance has its maximum value (devices with linear dependence of g_m vs. V_{gs}). A good starting point for V_{gs} and I_{pk} for such devices is the gate voltage at which $Ipk = 0.5I_{dss}/(1 + \lambda V_{ds})$, where I_{dss} is the saturated drain current. P_3 is responsible for the pinch-off characteristics of the device and P_2 makes the transconductance curve asymmetrical. The model equation and its derivatives are all well behaved which is important for a correct simulation of the harmonic generation. P_1 and V_{pk} can be considered constant, when the device is operating in the saturated region.

When I_{ds} is unsaturated (at small drain voltages), however, the transconductance, g_m, the corresponding gate voltage, V_{pk}, and the coefficient P_1 are dependent on V_{ds} (Figs. 1 and 2). At small drain voltages P_1 can be several times larger than P_{1sat}. For circuits like resistive mixers, attenuators and modulators, which are biased at low V_{ds}, and also for InP devices, which usually are also operated at small drain voltages, the dependencies of P_1 and V_{pk} on V_{ds} are important and those dependencies must be accounted for.

The types of functions, which can be used to describe dependencies of the V_{pk} and P_1, can be found by studying the derivatives of the drain current. The transconductance is equal to (if higher order terms of ψ are neglected)

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = I_{pk}P_1 \operatorname{sech}[P_1(V_{gs} - V_{pk})]^2(1 + \lambda V_{ds}) \tanh[\alpha V_{ds}]. \quad (3)$$

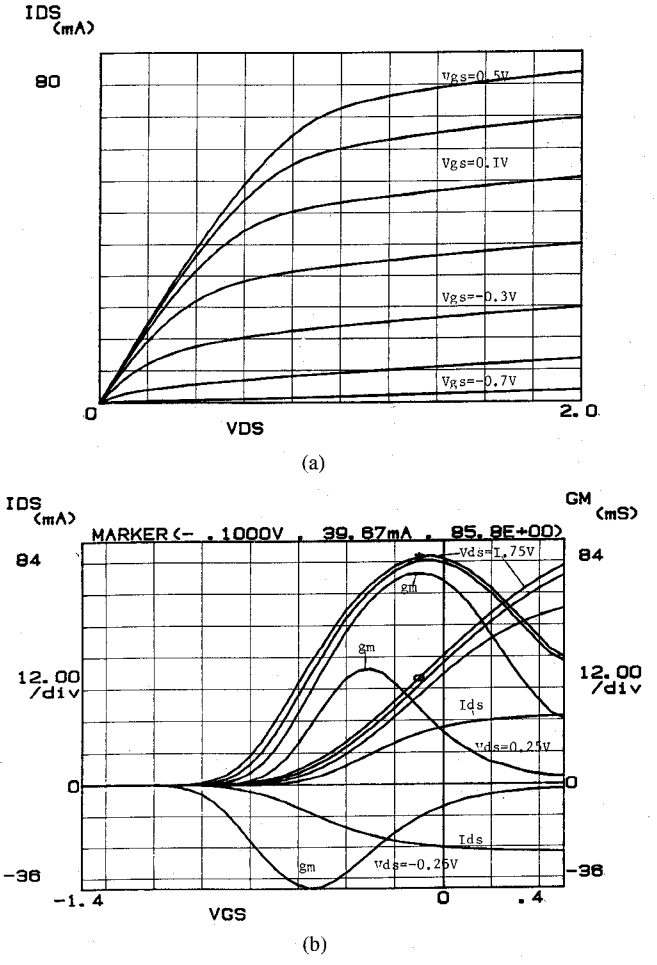

Fig. 1. DC-characteristics of ATF35076: (a) $I_{\rm ds}$ versus $V_{\rm ds}$ and $V_{\rm gs}$ ($V_{\rm gs}$:0.5 V: −0.7 V, step 0.2 V) and (b) $I_{\rm ds}$ and g_m vs $V_{\rm gs}$ and $V_{\rm ds}$ ($V_{\rm ds}$: −0.25 V: 1.75 V step 0.5 V).

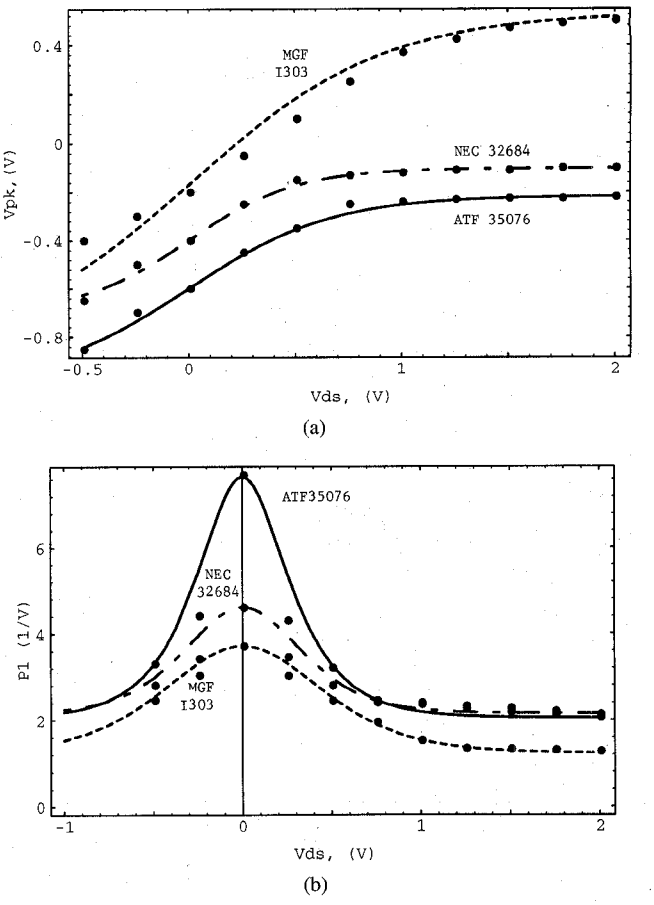

Fig. 2. Experimental and modeled dependencies of $V_{\rm pk}$ and P_1: (a) $V_{\rm pk}$ versus $V_{\rm ds}$: $V_{\rm pk} = -0.55 + 0.33 \cdot \text{Tanh}(1.7\,V_{\rm ds})$ (ATF3 5076), $V_{\rm pk} = -0.35 + 0.25 \cdot \text{Tanh}(2.7\,V_{\rm ds})$ (NEC 32684), $V_{\rm pk} = -0.16 + 0.73 \cdot \text{Tanh}(V_{\rm ds})$ (MGF1303B): (b) P_1 versus $V_{\rm ds}$: $P_1 = 2.1\ (1 + 2.6/\cosh^2(3.6\,V_{\rm ds})$ (ATF35076), $P_1 = 2.15(1 + 1.1/\cosh^2(3.2\,V_{\rm ds})$ (NEC32684), $P_1 = 1.23(1 + 1/\cosh^2(1.7\,V_{\rm ds})$ (MGF1303B).

The gate voltage $V_{\rm pk}$ at which we have maximum transconductance is dependent on the drain voltage and can be extracted by finding the gate voltages, at which the second derivative of the drain current is equal to zero. This can be done numerically, but it is much simpler to use the following simplified expression for $V_{\rm pk}$:

$$V_{\rm pk}(V_{\rm ds}) = V_{\rm pk0} + (V_{\rm pks} - V_{\rm pk0})(1 + \lambda V_{\rm ds})\tanh(\alpha V_{\rm ds}) \quad (4)$$

where $V_{\rm pk0}$ and $V_{\rm pks}$, is $V_{\rm pk}$ measured at $V_{\rm ds}$ close to zero and in the saturated region, respectively. In many cases $(1 + \lambda \cdot V_{\rm ds}) \approx 1$.

The drain-to-source current and transconductance is zero at $V_{\rm ds} = 0$. Hence, the ratio $g_m/I_{\rm ds}$ has a singularity as $V_{\rm ds}$ approaches zero and is not suited to model the P_1 dependency on the drain voltage in harmonic balance simulations. It is therefore better to use a simple function to describe the experimental P_1 dependency on drain voltage. A good fitting of P_1 and good results in harmonic balance simulations are obtained using the function

$$P_1 = P_{1\rm sat}\left[1 + \left(\frac{P_{10}}{P_{1\rm sat}} - 1\right)\frac{1}{\cosh^2(BV_{\rm ds})}\right] \quad (5)$$

where $P_{10} = g_{\rm m0}/I_{\rm pk0}$ at $V_{\rm ds}$ close to zero and B is a fitting parameter ($B \approx 1.5\ \alpha$). Equation (5) is an extension of our model, which takes into account the increase of g_m to $I_{\rm pk}$ ratio at small drain voltages. Similar $V_{\rm ds}$ dependence can also be seen for all the coefficients of the Ψ function for many transistors at low drain voltages.

The measured and modeled $I_{\rm ds}$ and g_m vs $V_{\rm gs}$ characteristics, for ATF35076 are shown in Fig. 3. Similar results were obtained for other devices. DC- and S-parameters of the packaged devices were measured in a Maury MT-950 transistor fixture and Wiltron 360/HP 8510 C VNA in the frequency range 0.1–18 GHz. We have used the equivalent circuit of the transistor shown in Fig. 4 to model the packaged transistors. The parasitic parameters L_g, L_d, L_s, R_g, R_d, R_s, C_p were fixed at the values extracted from the S-parameter measurement at $V_{\rm ds} = 0$. The component values of the small signal equivalent circuit of the cold FET were extracted using our own extraction program, but similar results were obtained using MDS (Hewlett Packard), Scout and Microwave Harmonica. (Compact Software). The frequency dispersion of transconductance and output conductance of the device [20]–[23] was investigated. The difference between DC transconductance and transconductance values extracted from S-parameters was very small (less than 10%). For the transistors where dispersion effects are significant, pulsed

TABLE I
EXTRACTED MODEL PARAMETERS

	Ipk (mA)	P_{1sat}	P_{10}	P_2	P_3	V_{pks} [V]	V_{pko} [V]	α	λ	K_g	R_s [Ω]	R_d [Ω]	R_g [Ω]	R_c [kΩ]	C_{gs} (pF)	C_{gd} (pF)	C_{rf} (pF)
NEC32684	41	2.15	4.6	-0.25	1.8	-0.1	-0.35	2.2	0.05	0.2	2	2.5	1.9	1.8	0.24	0.025	5
ATF35076	37	2.1	7.7	-0.2	3.5	-0.22	-0.55	1.7	0.03	0.20	2.2	2.7	2.2	3	0.2	0.035	5
FHX15	39	2.52	6.9	-0.5	3	0	-0.25	1.93	0.07	0.1	2	2.3	1.8	2	0.25	0.025	5
MGF4914D	42	2.95	6.9	-0.3	6.8	0.02	-0.45	3.3	0.04	0.15	1.8	2.2	1.7	1.0	0.3	0.027	5
MGF1303B	40	1.45	2.9	-0.3	0.75	0.23	-0.25	2.5	0.04	0.15	3.5	3.3	2.4	1.7	0.52	0.045	1

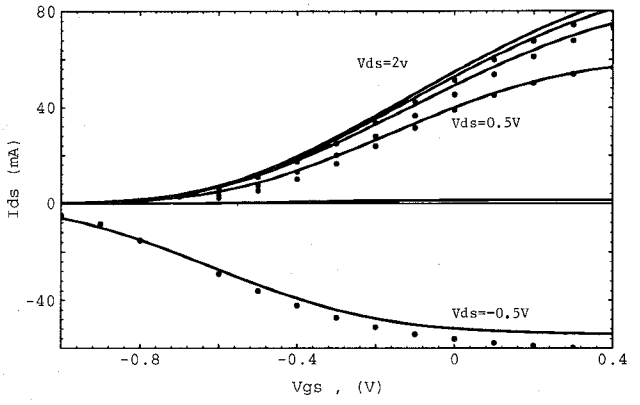

Fig. 3. Experimental and modeled of I_{ds}, and g_m versus V_{gs} for ATF35076: (a) I_{ds} versus V_{gs} and (b) g_m versus V_{gs}.

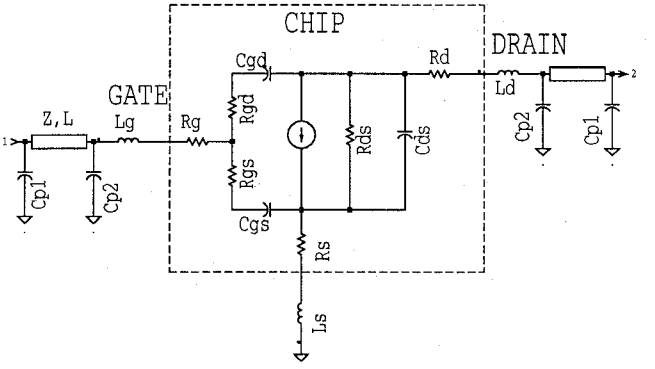

Fig. 4. Equivalent circuit of the packaged transistor ATF 35076. $Cp1$ = 0.18 pF, Cbp = 0.05 pF, w = 0.25 mm, L = 0.27 mm, Lg = 0.33 nH, Ld = 0.33 nH, Ls = 0.05 nH.

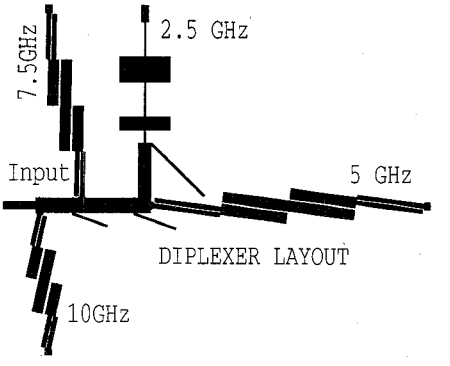

Fig. 5. Layout of the diplexer.

gate measurement [21] and pulsed S-parameters measurements [14] should be performed. An RC-series circuit was used to model low frequency dispersion of the output conductance. By adjusting the λ values extracted from DC measurement and the values of RC-circuit it was possible to fit both DC characteristics and S-parameters. Heating effects were found negligible for this small power devices for gate voltages smaller than 0.25 V, and drain current and voltages in the specified safety region. A junction model, which is available in the FET model of MDS (HP), was used to model the forward conduction characteristic of the Schottky diode of the HEMT. DC-parameters were measured using a HP 4145B parameter analyser (integration time 3.6 ms). Model parameters were extracted for packaged HEMT's and MESFET's manufactured by different manufactures. The values of I_{pk}, P_{1sat}, P_{10}, V_{pk0}, V_{pks}, α and λ were determined from DC measurements, taking into account the voltage drop over R_s and R_d. Usually, there is no need to adjust measured values of I_{pk}, P_{1sat}, P_{10}, V_{pk0}, and V_{pks}. The coefficients P_1, P_3 and P_2 were extracted from the function Ψ calculated from saturation current data (V_{ds} = 2 V), by using simple polynomial curve fitting. The coefficients, which describe the drain part of the I_{ds}-equation, α, λ, and K_g, were extracted in the ordinary way [16]. The best agreement between measured and simulated output power spectrum was obtained using the values of α and λ extracted from I-V characteristics at positive gate voltages (V_{gs} = 0.4 V). The process of the extraction of the model parameters is described in more detail in [24]. The extracted model parameters (Table 1) for some HEMT devices (NEC32684 (NEC), ATF35076 (Avantek), FHX15FA (Fujitsu), MGF4914D and a MESFET MGF1303B (Mitsubishi)) were used in Harmonic Balance Simulator (MDS from Hewlett Packard) to simulate the DC and microwave performance of those transistors.

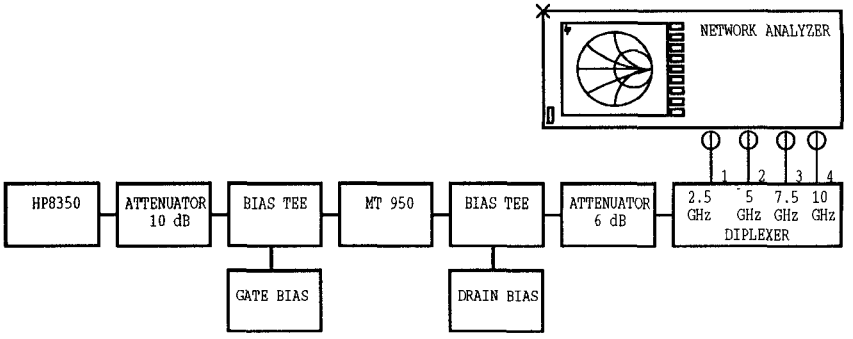

Fig. 6. Measurement setup.

The model has the following advantages:

1) The values of the model parameters, $I_{\rm pk}$, $V_{\rm pk}$, g_m, are directly coupled to measured values of the device. These values are well defined, as opposed to the usually used pinch-off voltage.
2) Derivatives are well defined. The functions have an infinite number of derivatives and harmonics, which are determined by $I_{\rm pk}$, $V_{\rm pk}$ and P_1.
3) Good accuracy of simulated $I_{\rm ds}$, S-parameters, generated harmonic spectrum and intermodulation products is reached using only three terms in the function Ψ. If for some reasons higher accuracy is required, more terms can be used in the function Ψ.

III. The Measurement Setup

In order to reduce the influences from incorrect modeling of the parasitics [7], [15] the measurements were performed at relatively low frequencies (fundamental frequency 2.5 GHz). The influence of the $C_{\rm gs}$ and $C_{\rm gd}$ models on the result of the simulations were investigated. Simulations was performed with different models: linear (constant), junction model and the model described in [11]. It was found that the simulated output power spectrum is not very sensitive to the capacitance models. Some difference was observed at the gate voltages for which the second and fourth harmonics have their minimum. The reason for this is that the fundamental-frequency component of the pumped transistor transconductance wave form is the dominant factor affecting the generated power spectrum. The largest difference in the simulations was found at the fourth harmonics: the linear model predicted much sharper minimas in the output power spectrum, compared to the other capacitance models. The nonlinear models of the capacitances were found to fit better the measurements. The difference in the simulation results between the junction capacitance model and the model of the capacitances described in [11] was less then 1 dB for the fourth harmonic and smaller for the 1st, 2nd, and 3rd harmonics. In this work we chose the built in internal junction model of MDS in order to decrease simulation time. The relative importance of the magnitude of $C_{\rm gs}$ and $C_{\rm gd}$ was also investigated. A simulation was performed with doubled $C_{\rm gs}$ and $C_{\rm gd}$ values, and the difference in the calculated output power spectrum was about 2 dB for the forth harmonic. In order to evaluate the influence of the nonlinear capacitance models it is necesary to measure at higher frequencies and perform on wafer measurements to reduce the uncertainties introduced by the parasitics of the packaged transistors or to use standard S parameter extraction procedure which is more convenient (10% change in $C_{\rm gs}$ value results in 5 degrees change in phase of S_{11} at 20 GHz).

TABLE II
Measured Performance of the Diplexer Filter

frequency	2.5 GHz	5 GHz	7.5 GHz	10 GHz
channel	S_{21} [dB]	S_{21} [dB]	S_{21} [dB]	S_{21} [dB]
2.5 GHz	-1.15	-30	-53	-39
5 GHz	-50.5	-1.8	-37	-50
7.5 GHz	-62	-40	-2.5	-52
10 GHz	-72	-61	-33	-1.7

In order to increase the speed and accuracy of the measurements of the power spectrum, a special diplexer, selecting each harmonic was designed and fabricated. It consists of a low pass filter for the fundamental and 3 bandpass filters for the second, third, and fourth harmonic (Fig. 5). The bandwidth of each channel is approximately 10%. The measured performance of the diplexer filter is shown in Table II. Measurement setup for the harmonics measurements is shown in Fig. 6. A low pass filter (f_c = 3 GHz) was added to the generator output to reduce harmonics generated by the sweeper. By using this type of set up, diplexer, filter and scalar network analyser, it is possible to make measurements simultaneously on all four channels, which increases the speed of the measurements. The losses and levels at different channels were calibrated using an Anritsu power meter (ML83A) and the accuracy of the measurements is better than 0.25 dB for the fundamental and better than 0.4 dB for the harmonics.

IV. Measurement Results and Comparison with the Model

In Figs. 7–9 simulated (lines) and measured (points) data are compared for the two packaged HEMT's and for a MESFET device. The maximum input power was set 3 to dBm. At higher input powers the gate is rectifying, and because of the self biasing, stability problems were encountered. MDS from Hewlett Packard was used for simulation. Similar results were obtained by using devices from other manufacturers (see Section II). The output power level at the first harmonic is mainly determined by the value of $I_{\rm pk}$ and transconductance g_m. The transconductance is by definition equal to $g_m = P_1 \cdot I_{\rm pk}$. The gate voltage at which we have minimum of the second and forth harmonic is fixed by $V_{\rm pk}$. All these parameters were

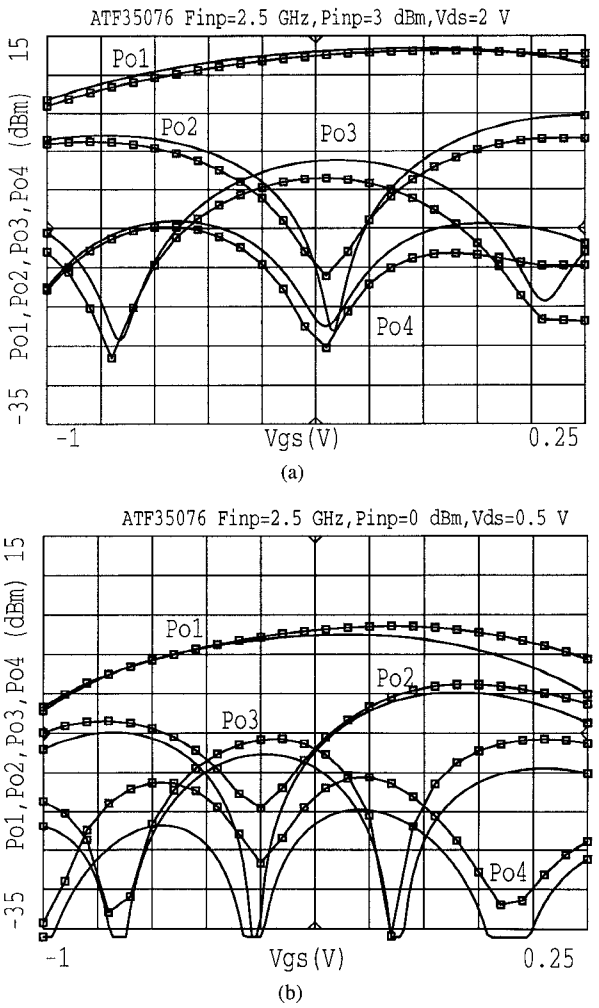

Fig. 7. Output power of ATF35076: (a) $P_{\text{in}} = 3$ dBm, $V_{\text{ds}} = 2$ V, and (b) $P_{\text{in}} = 0$ dBm, $V_{\text{ds}} = 0.5$ V.

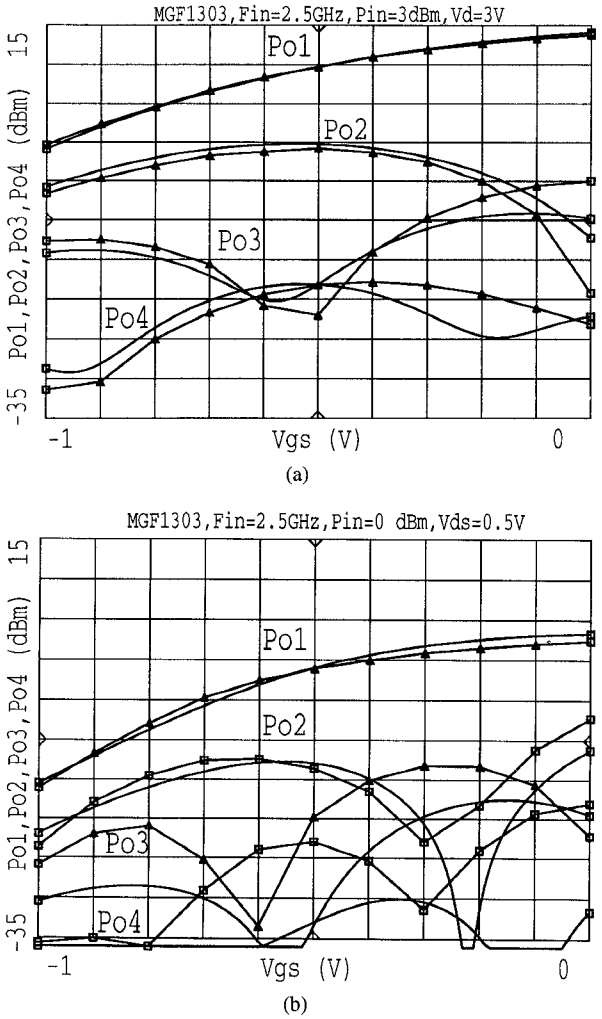

Fig. 8. Output power of MGF1303B: (a) $P_{\text{in}} = 3$ dBm, $V_{\text{ds}} = 3$ V, and (b) $P_{\text{in}} = 0$ dBm, $V_{\text{ds}} = 0.5$ V.

measured at DC with a very high accuracy. At the drain voltage for which the parameters of the model were extracted (2 V), the difference between simulated and generated first harmonic was less than 0.5 dB. The accuracy of the simulation for the second and higher harmonics is also good. The largest difference can be found in the region where V_{gs} is positive. This is probably due to conduction in the gate Schottky diode-according to the simulations, gate voltage reaches a value of $V_{\text{gs}} + 1$ V, at a power of 3 dBm. At low drain voltages, the simulated current I_{ds}, and the transconductance g_m are typically within 5% of the measured values. The extension of our model improved the agreement between measured and modeled output power spectrum at low drain biases. At high drain voltage (> 1 V), it is of less importance to modify the model.

The similar set up was used to check intermodulation products of HEMT devices. Signals from two generators ($f_1 = 1.00$ GHz, $f_2 = 1.01$ GHz) with equal power levels were combined with a power splitter. A Tektronix spectrum analyser was used to monitor the generated products. The measured and simulated bias dependence of the fundamental output power (P_{o1}), and the second (P_{im2}) (at 10 MHz) and third (P_{im3}) order intermodulation products at different input power levels are presented in Fig. 9(a) and (b). Simulated and experimental dependencies of fundamental output power and intermodulation products vs input power level is presented in Fig. 10. Since the accuracy of the simulation of the harmonics generated in the HEMT is good, there is a good agreement between measured and simulated intermodulation products. They are within a few dB of the measurement, which is similar to the measurement error.

V. Conclusion

The proposed nonlinear model describes the gate bias, drain bias, and input power dependencies of the output power spectrum well, at least to the fourth harmonic. The model can be used for predicting the performance of multipliers and mixers, including intermodulation simulations. The evaluation method by using a filter-diplexer is fast and convenient.

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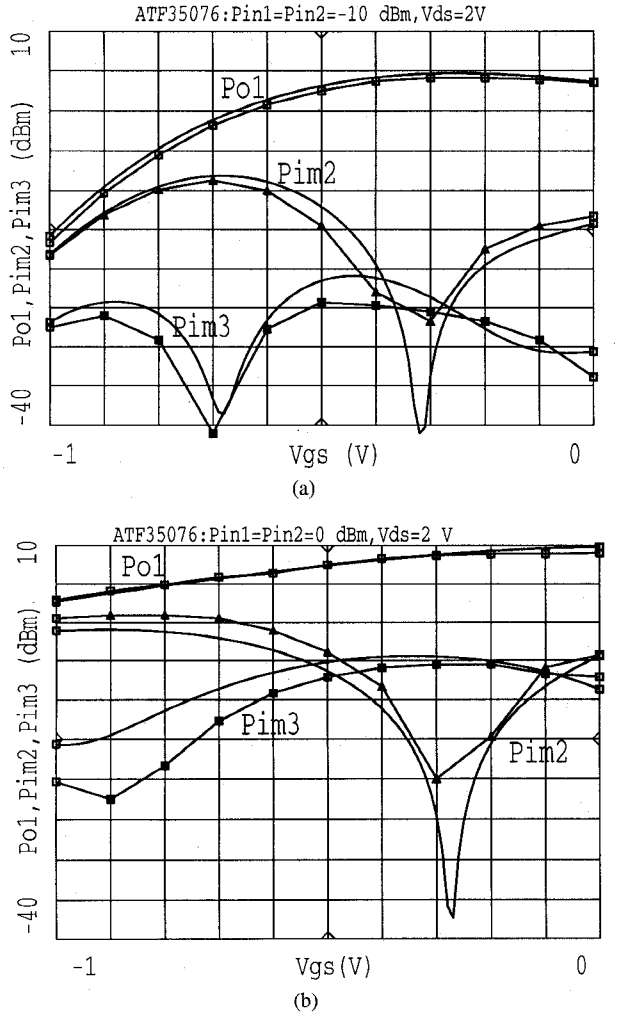

Fig. 9. Fundamental power output (P_{o1}), second (P_{im2}) and third (P_{im3}) intermodulation products versus gate voltage V_{gs} for ATF35076 ($f_{in1} = 1.00$ GHz, $f_{in2} = 1.01$ GHz, $P_{in1} = P_{in2}$, and $V_{ds} = 2$ V): $P_{in} = -10$ dBm (a) and $P_{in} = 0$ dBm (b).

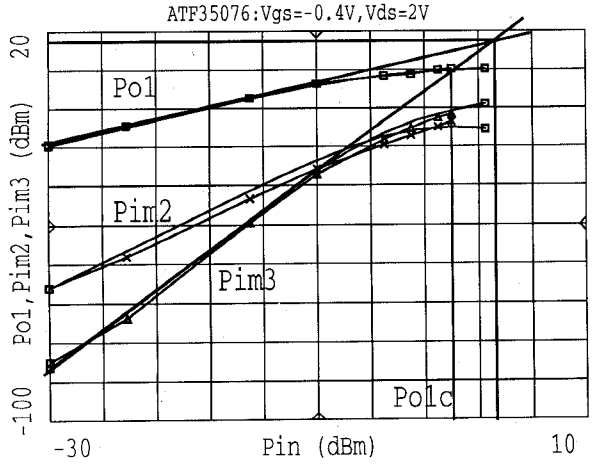

Fig. 10. P_{o1}, P_{im2}, P_{im3} versus input power P_{in}.

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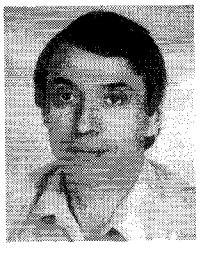

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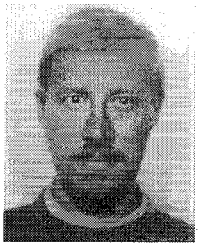

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